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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,877	HOLMBERG ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Amendment and Remarks filed on April 19, 2007 regarding application 10/511,877 filed on October 19, 2004.

2. Claims 1, 14-15, and 17 have been amended.

Claim 23 has been added.

Claim 13 has been cancelled.

Claims 1-12 and 14-23 are pending in the application under consideration.

3. ***Response to Amendments and Remarks***

Applicants' amendments and remarks have been fully and carefully considered. In response, a new ground of claim analysis based on a newly identified reference (Jensen et al., US 7,149,878) has been made. Refer to the corresponding sections of the following claim analysis for details.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-5, 7-12, 14, 17-21 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Jensen et al. (US 7,149,878).

It is noted that, in the following claim analysis, those elements recited by the claims are presented in **bold** font.

As to claim 1, Jensen et al. disclose **a computer system** [abstract] **comprising**: **a special-purpose register file** [the corresponding special-purpose register file is the Boundary Address register file (figure 5, 522; figure 6, 630; column 12, lines 33-59; column 15, lines 9-11)] **separate from other general register files of the computer system** [Additionally, contents of a general purpose register file (not shown) are accessed as prescribed by the program instruction within the decode/register stage(column 14, lines 8-11); column 14, lines 24-27)] **adapted solely for holding memory address calculation information received from memory** [column 15, lines 15-40; figure 6], **said special-purpose register file having at least one dedicated interface for allowing efficient transfer of memory address calculation information in relation to said special-purpose register file** [figures 5 and 6 show the interface between the special-purpose register file (i.e., the Boundary Address register file) and the memory (figure 5, 560); the address evaluation logic (figure 6, 621)];

means for determining a memory address in response to memory address calculation information received from said special-purpose register file, thus enabling a corresponding memory access [column 15, lines 15-40; abstract; figure 6; column 12, lines 33-59].

As to claim 2, Jensen et al. teach that **the computer system according to claim 1, further comprising means for effectuating a memory access based on**

the determined memory address [abstract; figure 6; column 15, lines 15-40; column 12, lines 33-59].

As to claim 3, Jensen et al. teach that **the computer system according to claim 1, wherein said at least one dedicated interface comprises a dedicated interface between said special-purpose register file and memory** [figures 5 and 6 show the interface between the special-purpose register file (i.e., the Boundary Address register file) and the memory (figure 5, 560); the address evaluation logic (figure 6, 621)].

As to claim 4, Jensen et al. teach that **the computer system according to claim 1, wherein said at least one dedicated interface comprises a dedicated interface between said special-purpose register file and said means for determining a memory address** [figures 5 and 6 show the interface between the special-purpose register file (i.e., the Boundary Address register file) and the memory (figure 5, 560); the address evaluation logic (figure 6, 621)].

As to claim 5, Jensen et al. teach that **the computer system according to claim 1, wherein said at least one dedicated interface includes a dedicated data path adapted in width to said memory address calculation information** [figures 5 and 6 show the interface between the special-purpose register file (i.e., the Boundary Address register file) and the memory (figure 5, 560); the address evaluation logic (figure 6, 621)].

As to claim 7, Jensen et al. teach that **the computer system according to claim 1, wherein said means for determining a memory address comprises at**

least one functional processor unit [the address evaluation logic (figure 6, 621) of the ISA mode controller (figure 6, 620)].

As to claim 8, Jensen et al. teach that **the computer system according to claim 7, wherein a forwarding data path is arranged from an output bus associated with said at least one functional processor unit to an input bus associated with said at least one functional processor unit** [figures 5 and 6 show the interface between the special-purpose register file (i.e., the Boundary Address register file) and the memory (figure 5, 560); the address evaluation logic (figure 6, 621)].

As to claim 9, Jensen et al. teach that **the computer system according to claim 1, wherein said means for determining a memory address is operable for executing special-purpose instructions in order to determine said memory address** [figure 6 shows that the address evaluation logic and the associated instructions; abstract; column 12, lines 33-59].

As to claim 10, Jensen et al. teach that **the computer system according to claim 1, further comprising means for executing special-purpose load instructions in order to load said memory address calculation information from said memory to said special-purpose register file** [column 12, lines 33-59].

As to claim 11, Jensen et al. teach that **the computer system according to claim 10, wherein said means for executing special-purpose load instructions comprises at least one functional processor unit** [the address evaluation logic (figure 6, 621) of the ISA mode controller (figure 6, 620); column 12, lines 33-59].

As to claim 12, Jensen et al. teach that **the computer system according to claim 11, wherein a forwarding data path is arranged from said memory to an input wherein said memory address calculation information is in the form of implicit memory access information** [figures 5 and 6 show the interface between the special-purpose register file (i.e., the Boundary Address register file) and the memory (figure 5, 560); the address evaluation logic (figure 6, 621); column 12, lines 33-59; the memory access information is in implicit form because the actual address is not directly contained in the instruction and needs to be derived by the address evaluation logic].

As to claim 14, Jensen et al. teach that **the computer system according to claim 23, wherein said implicit memory access information includes memory address translation information** [figure 6 shows that the address evaluation logic (figure 6, 621) translates the implicit memory access information (D0000000) into the actual address using the Boundary Address register file (figure 5, 522; figure 6, 630; column 15, lines 9-11; column 12, lines 33-59)].

As to claim 17, refer to "As to claim 1" presented earlier in this Office Action.

As to claim 18, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 19, refer to "As to claim 3" presented earlier in this Office Action.

As to claim 20, refer to "As to claim 4" presented earlier in this Office Action.

As to claim 21, refer to "As to claim 5" presented earlier in this Office Action.

As to claim 23, refer to "As to claim 12" presented earlier in this Office Action.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6, 15-17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 7,149,878), and in view of Aikawa et al. (US 5,371,865).

Regarding claim 6, Jensen et al. do not mention using a dedicated cache adapted for memory address calculation information.

However, Aikawa et al. disclose **a computer system** [Computer with Main Memory and Cache memory for Employing Array Data Pre-Load operation Utilizing base-Address and Offset operand (title); figures 4A and 4B] **comprising**:
a special-purpose register file [the Register File, figure 4B, 53] **adapted for holding memory address calculation information received from memory** ["$25" and "($4)" are supplied to register file 53 through line 55. The base address stored in register "$4" is read from register file 53 (column 7, lines 1-3)], **said special-purpose register file having at least one dedicated interface for allowing efficient transfer of memory address calculation information in relation to said special-purpose register file** [figure 4B shows a dedicated interface (50) between the data memory (32) and the register file (53)];

means for determining a memory address in response to memory address calculation information received from said special-purpose register file, thus enabling a corresponding memory access [The corresponding means is the ALU (figure 4B, 57); At the same time, ALU 57 adds the base address, which is received through line 59, to offset "64" which is received through selector 58. Then ALU 57 stores the addition result, which is a new base address, in register "$3" of register file 53 through line 60 (column 7, lines 13-17)].

Specifically, Aikawa et al. teach that **said memory comprises a dedicated cache adapted for said memory address calculation information** [A computer having a main memory for storing a plurality of data, a cache memory for temporarily storing a portion of the plurality of data, a processor for accessing data stored in the cache memory and processing the data according to instructions. The processor has an access instruction combined with a preload instruction, and an access instruction only for accessing data, and includes indicator circuitry for indicating a preload condition to the cache memory when the processor accesses data from the cache memory according to the access instruction combined with the preload instruction. The cache memory preloads data to be accessed next by the processor from the main memory when the processor indicates the preload condition (abstract)].

It is well known in the art that using a cache memory reduces memory access latency and increases the throughput.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize the benefits of using a cache memory, as is

well known in the art and further demonstrated by Aikawa et al., and to incorporate it into the existing apparatus disclosed by Jensen et al., to reduce memory access latency and to increase the throughput.

As to claim 15, refer to "As to claim 1" and "As to claim 6" presented earlier in this Office Action.

Further, Jensen et al. teach **means for determining a memory address in response to memory access information received from said special-purpose register file over a second dedicated interface** [figures 5 and 6 of Jensen et al.; one interface at the input port of the register file and another interface at the output port of the register file].

As to claim 16, Jensen et al. teach that **the computer system according to claim 15, wherein said first and second dedicated interfaces are adapted in width to said memory address calculation information** [figures 5 and 6 show the interface between the special-purpose register file (i.e., the Boundary Address register file) and the memory (figure 5, 560); the address evaluation logic (figure 6, 621)].

As to claim 22, refer to "As to claim 6" presented earlier in this Office Action.

9. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis in this Office Action.

- Morris et al., (US 6,631,460), "Advanced Load Address Table Entry Invalidation Based on Register Address Wraparound."
- Baror et al., (US 4,926,323), "Streamlined Instruction processor."

- Henry et al., (US 6,862,670), "Tagged Address Stack and Microprocessor Using Same."

Conclusion

10. Claims 1-12 and 14-23 are rejected as explained above.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

May 16, 2007

PIERRE BATAILLE
PRIMARY EXAMINER
5/17/07